

Serial No. 10/709,325  
Docket No. BUR920030184US1 (BUR.107)

**AMENDMENTS TO THE CLAIMS:**

(It is noted that there are no new claim amendments, but the version below is provided for reference and for convenience of the USPTO)

1. (Previously presented) An electronic chip, comprising:
  - a first circuit design module having a first grid; and
  - a second circuit design module having a second grid,wherein said first grid and said second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in a fabrication of said electronic chip, such that said first grid and said second grid do not accumulate an excessive differential voltage due to said plasma process.
2. (Original) The electronic chip of claim 1, wherein at least one of said first grid and said second grid comprises a metallization grid.
3. (Previously presented) The electronic chip of claim 1, wherein said first grid and said second grid respectively comprise one of a power grid and a ground grid.
4. (Previously presented) The electronic chip of claim 1, wherein said first grid and said second grid are interconnected by at least one of:
  - a diffusion region;
  - a gate of a field effect transistor;
  - a source of a field effect transistor connected to said first grid and a drain of said field effect transistor connected to said second grid;

Serial No. 10/709,325  
Docket No. BUR920030184US1 (BUR.107)

a local interconnect; and  
a metallization layer that is designed to electrically interconnect at a boundary of said first circuit design module and said second circuit design module.

5. (Previously presented) The electronic chip of claim 1, wherein an interconnect between said first grid and said second grid is conductive during said plasma processing and is non-conductive during an operation of said chip unless activated by a signal.

6. (Original) The electronic chip of claim 1, wherein said chip comprises components fabricated in a layer that has substantially no leakage of carriers to a substrate of said chip.

7. (Original) The electronic chip of claim 6, wherein said chip includes a silicon on insulator (SOI) structure.

8. (Original) The electronic chip of claim of claim 6, wherein said layer is temporarily activated by said plasma processing such that carriers in said layer are migratable during said plasma processing.

9. (Original) The electronic chip of claim 2, wherein at least one of said first grid and said second grid comprises a metal grid that includes a predetermined surface area of at least one of said first circuit design module and said second circuit design module.

Serial No. 10/709,325

Docket No. BUR920030184US1 (BUR.107)

10. (Original) An electronic apparatus comprising:

an electronic chip fabricated in accordance with claim 1.

11. (Withdrawn) A method of at least one of designing an electronic chip and fabricating said electronic chip, said method comprising:

interconnecting at least one grid of a design module of an electronic circuit formed on said chip with a corresponding grid in a second design module in a stage of fabrication of said chip such that a plasma processing of said fabrication does not cause a differential charge that damages a component of said chip..

12. (Withdrawn) The method of claim 11, wherein at least one of first grid and said second grid each comprise a grid formed by metallization.

13. (Withdrawn) The method of claim 11, wherein said first grid and said second grid comprise one of a power grid and a ground grid.

14. (Withdrawn) The method of claim 11, wherein said first grid and said second grid are interconnected by at least one of:

a diffusion region;

a gate of a field effect transistor;

a source of a field effect transistor connected to said first grid and a drain of said field effect transistor connected to said second grid;

a local interconnect; and

Serial No. 10/709,325  
Docket No. BUR920030184US1 (BUR.107)

a first metallization layer that is designed to electrically interconnect at a boundary of said first circuit design module and said second circuit design module.

15. (Withdrawn) The method of claim 11, wherein said chip comprises components fabricated in a layer that has substantially no leakage of carriers to a substrate of said chip.

16. (Withdrawn) The method of claim 15, wherein said chip comprises a silicon on insulator (SOI) structure.

17. (Withdrawn) The method of claim of claim 11, wherein said layer is temporarily activated by said plasma processing such that carriers in said layer are migratable during said plasma processing.

18. (Withdrawn) The method of claim 12, wherein at least one of said first grid and said second grid comprises a metal grid that is a predetermined surface area of at least one of said first circuit design module and said second circuit design module.

19. (Original) An electronic apparatus comprising:

at least one electronic chip, comprising:

a first circuit design module having a first grid;

a second circuit design module having a second grid; and

Serial No. 10/709,325  
Docket No. BUR920030184US1 (BUR.107)

means for electrically interconnecting said first grid and said second grid no later than a first metallization layer that accumulates a charge during a plasma process in a fabrication of said chip.

20. (Original) The electronic apparatus of claim 19, wherein at least one of said at least one electronic chip comprises a chip including a silicon on insulator (SOI) structure.